AMENDMENT TO THE SPECIFICATION

Amend the paragraph beginning at page 3, line 22 as follows:

Clock generator 110 generates an output 116 having a frequency that is a multiple, m, of the frequency of a reference clock, REFCLK 112. In the illustrated embodiment, clock generator 110 is a phase locked loop (PLL). The PLL has a feedback path including inverter 182 172, divider 170, and flip-flop 150.

Amend the paragraph beginning at page 8, line 21 as follows:

Figure 5 thus illustrates a clock generator providing a clock output <u>514</u> having a frequency that is twice that of a received reference clock <u>512</u>. A multiplexer <u>530</u> is coupled to select one of the clock output <u>514</u> and a gated clock <u>520</u> output as a double clock <u>516</u> in accordance with a halt multiplexer control <u>546</u>. Divider circuitry <u>570</u> divides the double clock to provide an alignment signal <u>576</u> with a frequency half that of the double clock. A recovery circuit <u>598</u> recovers a first clock <u>580A</u> and a second clock <u>590A</u> from the double clock <u>516</u> in accordance with the alignment signal <u>576</u>, wherein the first and second clocks have substantially a 90° phase difference.

Amend the paragraph beginning at page 8, line 30 as follows:

The halt control should be disabled during normal operation. This is accomplished in one embodiment by tying HALT 542 to a logic level that ensures halt multiplexer control 546 always selects PLL output 514 during normal operational modes. Stop level 544 indicates the logic level at which the halt should occur as further described with respect to Figure 6.

Amend the paragraph beginning at page 11, line 6 as follows:

The integrated circuit die 830 resides within an integrated circuit package 820. A REFCLK <u>812</u> is provided to the clock generator 830 via an external pin 822 of the integrated circuit package 820.

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